Abstract—In this paper, a 18 GHz Low Noise Amplifier (LNA) is proposed with using 130 nm technology. In the designed LNA, the structure of one-stage cascode amplifier with source inductive degeneration is used. It operates with a 1.2 V power supply drawing a current of 12 mA. The LNA demonstrates 17.62 dB for S21 and 18.6 dB for MAG at the peak gain frequency of 17.49 GHz. The simulation results show that the proposed LNA has a minimum noise figure (NF) of 1.8 dB in the whole 3 dB bandwidth of 16.33-18.93 GHz. For large input signal level, P1dB, OIP3, and IIP3 are -14 dBm, +18 dBm and +1 dBm, respectively.

Index Terms— Low Noise Amplifier (LNA), Maximum Available Gain (MAG), Input third order Intercept Point (IIP3).

I. INTRODUCTION

Today, the advances in CMOS technology have guided the progress in the wireless communications circuits and systems area. Various new communication standards have also been developed to accommodate a variety of applications at different frequency bands. The modern wireless technology is motivated by the global trend of developing technology for low-cost and multifunction transceivers. One of the challenging building blocks in receivers is the low noise amplifier (LNA) [1]. The LNA contributes most of the noise figures. Therefore, the design and optimization in the noise figure, gain, and power consumption for a CMOS LNA becomes the major concern in millimeter-wave Integrated Circuits. In the conventional designs, the common-source configuration is usually used to implement a CMOS LNA. In order to make the best trade-off between the maximum small signal gain and the minimum noise figure, the inductive source degeneration structures [2] were reported. However, a single-stage common-source LNA cannot provide high gain, especially in millimeter-wave bands (MMW) [3]. In some reported papers, the LNAs with the cascode device. [4]-[8] become common. The cascode structure is composed of a common-source and a common-gate transistor. It has the advantages of high gain and good performance, as the operation frequency increases to MMW bands, the common-gate stage will contribute a considerable noise, and thus results in high noise figure of a cascode or triple-cascode structure in MMW LNA design. In another report [9], the parallel resonant inductor was used to reduce the noise of the cascode device, but a large inductor and bypass capacitor were required [3]. Our focus was in 20 GHz frequency that is reported in [11]-[18], but not in the same technologies. Among them, the single-structure has been used in [12]-[17], whereas the differential topology has been adopted in [11] and [18]. The inductive degeneration at the source of the input transistor has been used previously [11]-[12], [15]-[17] to achieve both noise and input impedance matching. To obtain high gain, the multi-stage configuration has been proposed [11], [13]-[17], however, they generally consume more power and lose the linearity performance. Generally, the single-structure has the advantage of a good noise figure (NF) and low-power consumption [19]. In the work reported by Wang et al [19], a 23 GHz one stage cascode source inductive degeneration LNA has been designed and fabricated in 45 nm planar bulk CMOS technology with high-Q above-IC inductors. It has the advantages of low power consumption, but its gain is weak and noise figure of 4 dB that is more than usual.

In this work, a one-stage cascode LNA with source inductive degeneration is designed. This is adopted to achieve low power dissipation, high linearity, suitable S-parameter and good noise figure. The calculated LNA figure of merit of 15.8 makes it suitable among the CMOS LNAs reported in this frequency range of operation. Simulation results show that the proposed LNA has a minimum noise figure of 1.8 dB in the whole 3 dB bandwidth of 16.33-18.93 GHz. It also indicates that the input reflection coefficient (S11), is less than -10 dB (-12.84 dB), the output reflection coefficient (S22) is -8.48 dB and the reverse reflection coefficient (S12), is about -30 dB. By employing the signal flow theory and the S-parameter, it is found that the low noise amplifier is unconditionally stable, because of Rollet’s Factor. Maximum available gain (MAG) and maximum stable gain (MSG) are 18.6 dB and 23.75 dB in the frequency of 17.49 GHz. For this design, P1dB, output third-order intercept point (OIP3) and input third-order
intercept point (IIP3) are -14 dBm, +18 dBm and +1 dBm, respectively (All in 17.49 GHz frequency).

This paper is organized as follows. Section II describes design techniques of LNAs. Section III presents the proposed one stage cascode LNA. Section IV addresses simulation results and at last we point conclusion in section V.

II. THE DESIGN TECHNIQUES OF LNAs

Impedance matching is by far one of the most important issues for any LNAs design. It is necessary for a circuit requiring high gain. High performance circuits mandate impedance matching within a narrow frequency band, and assuming ideal element, the loss-less impedance matching is possible by using a reactive element such as an inductor, a capacitor or a transmission line. Transmission lines, which have distributed properties are used for operating frequencies above 10 GHz and into the 100 GHz. Lumped elements such as inductors and capacitors can be used for frequencies between 1 GHz and 30 GHz. For frequencies lower than 1 GHz, purely active circuit’s topologies are preferred, since the area consumed for the lumped elements or transmission lines is too large and thus too costly. Impedance matching and reduction of reflections can be easily achieved by adding resistors in series or in parallel. However, in this case significant resistive losses would result, which cannot be acceptable for low power applications, where the signal has to be preserved as much as possible. In addition, matching resistors generate considerable noise. Low noise amplifiers have to provide source and load impedance, which are acceptable within the full bandwidth. Thus, resonant impedance matching is not feasible. From a system point of view, the sub-frequency range with the lowest performance is relevant. Gain and bandwidth (BW) have to be trade-off against one another. A reasonable figure of merit (FOM) for multipurpose amplifiers is given by [20]:

\[
FOM = \frac{BW [GHz]}{f_t [GHz]} \frac{S_21 [dB]}{NF [dB]} \frac{P_{1dB} [mW]}{P_{dc} [mW]} 
\]

The first term in Eq.(1) describes the bandwidth with respect to the ft of the used technology, the second factor considers the gain to noise figure ratio and the third term relates the large signal properties presented e.g. by the 1 dB compression point P1dB with the consumed DC power Pdc. The significance of the terms depends on their applications. Several modifications of Eq. (1) can be found in the literatures. Optionally, the representation of the large signal properties by means of the IIP3 instead of the P1dB may be also reasonable. Logarithmic as well as non-logarithmic measures may be applied.

A number of LNA topologies have been proposed to achieve the highest performance i.e. the cascade, the cascode [3], current reused [21], common-source with inductive source degeneration, common-source with resistive drain gate feedback and transformer folded-cascode [10]. All of these designs compromise between gain and performance. For example in cascode amplifiers gain is very high but there is no suitable stability or even chip area is large. In the design with an inductive source degeneration, we have low noise and high gain but stability can be critical for non-differential topologies due to undesired feedbacks in grounds [20].

A folded-cascode LNA, which has no cascode transistor, is one of the best choices for low voltage operations because it requires a supply voltage for only one drain saturation voltage (VDD>VDS,sat), whereas in Cascode amplifiers (VDD>2VDS,sat) to operate in linear region, it but it requires more inductive, which leads to an increase in a chip area. With employing transformer in a folded-cascode design, we can reduce the area of the inducers and improve the noise performance of the LNA by decreasing the contribution from the noise of common-gate stage [10].

III. THE PROPOSED ONE STAGE CASCODE LNA

The circuit diagram of the designed one-stage source inductive degeneration LNA is shown in Fig. 1. The cascode amplifier formed by M2 and M1 is employed to reduce the Miller effect of M2 and to obtain good reverse isolation. The degenerative inductor Ls at the source of M2 is used to provide the input more resistive and low ohmic for impedance matching. With Ls, the design goals of both noise and input impedance matching can be performed simultaneously. Furthermore, Ls does not seriously degrade the NF performance. However, increasing the value of Ls reduces the gain of the amplifier. The value of Ls in this design is set at 0.08 nH. The widths of M1 and M2 are chosen as 88.6µm and 34.3 µm. The power consumption is designed to be less than 13 mW from a 1.2 V power supply.
Fig. 2. Simplified equivalent small signal circuit

The voltage gain of this circuit is calculated as:

\[ A_v = \frac{V_o}{V_i} = \frac{C_3}{C_3 + C_4} \times \frac{L_d S}{B(S)} \]  

(2)

B(S) is expressed as follows:

\[ B(S) = D(S) + L_s S \quad \Rightarrow \quad B(S) = \frac{1}{g_m^2 + C_{gs}^2 S^2} + L_s S \]  

(3)

\[ D(S) = \left( \frac{1}{g_m^2 + C_{gs}^2 S^2} \right) \]  

(4)

\[ B(S) = \frac{1 + g_m^2 + C_{gs}^2 S^2}{g_m^2 + C_{gs}^2 S^2} \]  

(5)

Table I shows the design values of the proposed LNA.

**TABLE I. DESIGN VALUES OF THE LNA**

<table>
<thead>
<tr>
<th>Transistor size</th>
<th>(W/L)</th>
<th>(W/L)</th>
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<tbody>
<tr>
<td></td>
<td>(88.6/0.13)</td>
<td>(34.3/0.13)</td>
</tr>
<tr>
<td>Inductor value</td>
<td>L_d</td>
<td>L_s</td>
</tr>
<tr>
<td>----------------</td>
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<td>-----</td>
</tr>
<tr>
<td>0.5 nH</td>
<td>0.08 nH</td>
<td>0.665 nH</td>
</tr>
<tr>
<td>Capacitor value</td>
<td>C_1</td>
<td>C_2</td>
</tr>
<tr>
<td>62</td>
<td>19</td>
<td>76</td>
</tr>
</tbody>
</table>

The output-matching network has been designed to match 50 by L_d, C_3 and C_4. The bypass capacitors is added between V_g (V_DDD) and ground in order to stabilize the bias voltage (supply voltage) and to isolate the bias (supply) noise from entering the LNA.

IV. SIMULATION RESULTS

The proposed LNA shown in Fig. 1 is designed in a 0.13µm standard RFCMOS technology. The simulation of this LNA is performed with the advanced design system (ADS) tools. This LNA is operated with a 1.2 volts power supply drawing a current of 12 mA. Figure 3 shows the noise figure (NF) of LNA which varies from 1.77 dB to 2.2 dB in the whole bandwidth. Figure 4 indicates that the input reflection coefficient (S11), is -12.84 dB and the output reflection coefficient (S22), is -8.48 dB.

As seen in Fig. 5, The LNA has demonstrated 17.62 dB gain for forward transmission coefficient (S21) at the peak gain frequency of 17.49 GHz with the 3-dB bandwidth spans from 16.33-18.93 GHz. Figure 6 shows the reverse reflection coefficient (S12), that is about -30 dB. Stability is a very important issue for the LNAs. If low noise amplifiers is not stable, it would become useless since major properties including bandwidth, gain, noise, linearity, DC power consumption and impedance matching can be significantly degraded. For this design, there is a good stability (unconditionally stable) by employing the signal flow theory and S-parameter, which show the Rollet’s factor, given by [22]:

\[ K = \frac{1 + \| \Delta \|^2 - |S_{11}|^2 - |S_{22}|^2}{2 |S_{11}| |S_{22}|} \]  

(6)

Where \( \Delta = S_{11} S_{22} - S_{12} S_{21} \)

The unconditional stability requirement of LNA is (K > 1) and (|\( \Delta \| < 1 \)). It is shown in Fig. 7.
The maximum transducer power gain that is denoted proportion between real power in the load and the available source power achieved at optimum source and load termination and under stable conditions is called maximum available gain (MAG) that is given by [22]:

$$\text{MAG} = \frac{S_{21}}{S_{12}} \left[ K - \sqrt{K^2 - 1} \right]$$

The MAG is defined for (K>1). In Fig. 8, MAG is illustrated.

Linearity of a circuit is determined by a factor called third-order intercept point (IP3) and used as the input IP3 (IIP3) or the output IP3 (OIP3). They are useful parameters to predict low-level intermodulation effects. Figure 9, indicates this factor.

For this case, IIP3 and OIP3 are around 1 dBm and 18 dBm. Finally, simulated 1-dB compression point (P_{1dB}) is about -14 dBm. It is shown in Fig. 10.

To characterize the performance of all LNA, the FOM defined in Eq.(1) has been used with some changes. The modified FOM is as follows:

$$\text{FOM} = \frac{F_{\text{GHz}} |S_{21}| [dB]}{N \text{F}[dB] P_{dc} [mW]}$$

As seen in Table II, the LNAs in [14] and [18] have better gains and in [11] and [13] have better linearity performances than this work at the cost of higher power consumption for the first group and the cost of worse gain for the second group.
V. CONCLUSION

A 18 GHz, low noise amplifier (LNA) has been designed using 130 nm technology. In the designed LNA, the structure of one-stage cascode amplifier with source inductive degeneration is used. These simulation results show that the proposed LNA has a minimum noise figure (NF) of 1.8 dB in the whole 3 dB bandwidth of 16.33 - 18.93 GHz. By employing the signal flow theory and the S-parameter, it was found that, the Low Noise Amplifier is unconditionally stable because of Rollet’s factor that is greater than one. This design operates with a 1.2 volts power supply drawing a current of 12 mA. The LNA has demonstrated 17.62 dB for S21 at the peak gain frequency of 17.49 GHz. For this circuit, P1dBm, OIP3, and IIP3 are 20 dBm, 14 dBm, and 14 dBm, respectively.

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REFERENCES


